Hall Ticket Number:

Code No. : 15401 S

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

B.E. (ECE: CBCS) V-Semester Supplementary Examinations, May-2019

Integrated Circuits and Applications

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. Define slew rate and write its significance.
2. State the requirements of a good instrumentation amplifier?
3. Draw the circuit diagram of Schmitt trigger using 555 Timer.
4. Design a second order Butterworth low pass filter for cutoff frequency of 1.5KHz.
5. Find the resolution of 8-bit DAC for full scale output voltage of 10V.
6. Draw the circuit diagram of 2-bit parallel type ADC.
7. List salient characteristics of digital integrated circuits.
8. What is the drawback of open collector configuration? How it eliminated in Tristate logic?
9. Design a mod-10 Johnson counter.
10. Write the differences between static RAM and Dynamic RAM.

Part-B (5 × 10 = 50 Marks)

11.a) Describe the operation of ideal integrator with the help of circuit diagram and give its applications. [6]

b) Design an op-amp based application circuit to get an output voltage $V_0 = 5V_1 - 2V_2 - 3V_3$ [4]

12.a) Explain the functional diagram of 8038 and also derive the expression for frequency of oscillation. [6]

b) Design a PLL circuit using IC565 for a free running frequency of 400KHz and capture range of ±10 KHz with a supply voltage of ±6V. [4]

13.a) Describe the working of Dual Slope ADC with a neat circuit diagram. [6]

b) For 4-bit Dual slope ADC, consider R=100KΩ, C=1μF, clock frequency is 10 KHz, V_{ref} =-6V and V_{in} =3V. Determine the output count and conversion time after the conversion is completed [4]

14.a) Draw the circuit diagram of three input CMOS NAND gate and explain its operation. [5]

b) Design a BCD adder using IC 7483. [5]

15.a) Describe the principle of operation of parallel in serial out shift register and give its applications. [5]

b) Implement the logic function $F_1(a,b,c)=\sum(1,3,5,7)$ and $F_1(a,b,c)=\sum(0,2,3,7)$ using PAL and PLA [5]

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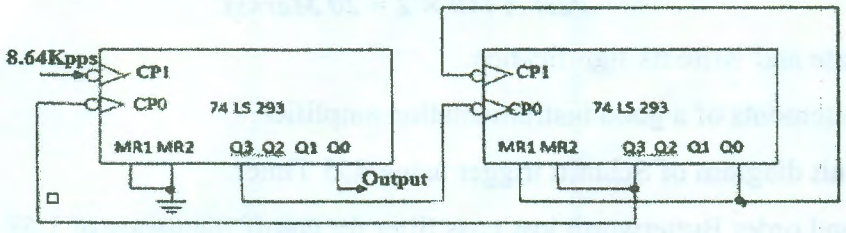
16.a) Design a 5V voltage regulator using IC723 for load current of 600mA under short circuit condition. [5]

b) Design a Narrow BSF to meet the following specifications: f_c = 2KHz, Q=20 and A_F =10. [5]

17. Answer any ***two*** of the following:

a) Determine the frequency at the output of the following circuit. [5]



b) Explain the working of 3-bit R-2R ladder type DAC. [5]

c) Compare the key characteristics of TTL, ECL and CMOS logic families. [5]